TITLE OF THE INVENTION

METHOD OF GENERATING ASIC DESIGN DATABASE

BACKGROUND OF THE INVENTION

The present invention relates to a method of generating an ASIC design database, which is important when a large-scale integrated circuit device such as a system LSI is to be designed.

There is known a conventional design method, which uses a database in order to avoid useless repetition at the time of re-designing or disability of design, when a system LSI is to be developed.

In designing an ASIC (Application Specific Integrated Circuit), a designer first analyzes given design specifications, examines architecture candidates, selects a most prospective architecture, and describes the selected architecture using a hardware description language. The act of the describing is called "operation description". The obtained operation description is an operation-level design result. The operation-level design is verified by applying an operation-level simulator or a verifier to this operation-level design result.

Based on the operation description, the designer then produces an RTL (Register Transfer Level) description in which the object of design is described in a register transfer level. The RTL description is automatically generated from the operation description

by means of an operation synthesis tool. The generated RTL description is also based on a hardware description language (HDL). The RT level design is verified by applying an RT level simulation tool, etc. to the RTL description.

Following the verification, a net list (gate-level logic circuit description), in which the object of design is described in a gate level on the basis of the RTL description, is generated by means of a logic synthesis tool. The gate-level design is verified by applying a logic simulation tool, etc. to the net list, following which a floor plan is carried out. In the floor plan for the net list, blocks constituting gate-level logic circuits are generally arranged and wired.

Subsequently, based on the result of the floor plan, the gate-level design represented by the net list is evaluated. Specifically, using the information on the arrangement of blocks constituting logic circuits and the information on the wiring of the blocks, the layout area, timing, power consumption, etc. are calculated.

In general, when the data mentioned above is stored, it is divided into specification data and RTL description data.

The specification data contains data on the process time, layout area, power consumption, test cost, etc.

The RTL description data is an RTL description file in units of an entity.

In the methods of constituting the databases, it is necessary to perform a process for extracting the content of specifications after the design is finished. This results in useless procedures in constituting the database.

BRIEF SUMMARY OF THE INVENTION

The object of the present invention is to provide a method of generating an ASIC design database, the method being capable of generating a database necessary for re-use design and efficient information collection, which are necessary when a large-scale integrated circuit device such as a system LSI is to be designed.

In order to achieve the object, the present invention may provide a method of generating an ASIC design database, comprising: extracting, when a function design using description data comprising a header portion and an entity portion has been performed, information necessary for reuse design from various execution results of the entity portion; writing the extracted information necessary for reuse design in the header portion of the description data; and storing, as one file at a predetermined location, the description data comprising the header portion in which the information necessary for reuse is written, and the entity portion.

Additional objects and advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed out hereinafter.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate presently preferred embodiments of the invention, and together with the general description given above and the detailed description of the preferred embodiments given below, serve to explain the principles of the invention.

FIG. 1 is a block diagram schematically showing the structure of an IC design support apparatus according to the present invention;

FIG. 2 is a flow chart illustrating the generation of a database and operations for collecting information;

FIG. 3 shows an example of a function design using RTL description;

FIG. 4 shows an example of a simulation result;

FIG. 5 shows an example of an analysis support (area information);

FIG. 6 shows an example of an analysis report

(timing information); and

FIG. 7 shows an example of a power consumption calculation result.

DETAILED DESCRIPTION OF THE INVENTION

An embodiment of the present invention will now be described with reference to the accompanying drawings.

FIG. 1 schematically shows the structure of an integrated circuit design support apparatus according to an ASIC design database generating method of the present invention. The hardware of this IC circuit design support apparatus is a computer system such as a work station.

The IC design support apparatus comprises a CPU 1, a ROM 2, a RAM 3, a memory 4, a hard disk drive (HDD) 5, a display 6, a keyboard 7, a mouse 8, and a printer 10.

The CPU 1 controls the entirety of the apparatus.

The ROM 2 stores control programs, etc.

The RAM 3 temporarily stores data.

The memory 4 stores data mentioned below.

The hard disk drive (HDD) 5 is a database to be reused for ASIC design, as will be described below in detail. The HDD 5 stores software tools, i.e. a simulation tool 5a, a logic synthesis tool 5b, a timing analysis tool 5c, a logic simulation tool 5d and a power consumption calculation tool 5e, which are executed by the CPU 1.

The display 6 displays various information.

The keyboard 7 and mouse 8 function as input devices.

The printer 10 performs a print-out operation as a printing apparatus.

As regards the above-described structure, the generation of a database and operations for information collection using the IC design support apparatus will now be described with reference to a flow chart of FIG. 2.

When a function design by RTL description made in a register transfer level has been carried out using HDL (VHDL, VERILOG) language, the CPU 1 of the IC design support apparatus executes simulation by means of the simulation tool 5a stored in the HDD 5 (ST1).

FIG. 3 shows an example of the function design by RTL description according to the present invention. The RTL description in this invention comprises a header portion and an entity portion. The RTL description is written in the HDD 5 as a reuse design database.

The CPU 1 generates a simulation result list (ST2). In this case, the list may be printed out by the printer 10 or displayed on the display 6.

FIG. 4 shows an example of a simulation result. In FIG. 4, "#799996" represents a simulation time.

The CPU 1 extracts the simulation time (step) from

the simulation result list and writes it in the header portion of the executed RTL description (ST3). The simulation time "#799996" nS shown in FIG. 4 is written in the header portion of the RTL description shown in FIG. 3.

Subsequently, the CPU 1 inputs the entity portion of the RTL description to the logic synthesis tool 5b and executes logic synthesis (ST4), and outputs a gate-level net list (ST5).

The CPU 1 inputs the net list to the timing analysis tool 5c and executes a timing analysis (ST6), and outputs an analysis report as an analysis result (ST7). In this case, the analysis report may be printed out by the printer 10 or displayed on the display 6.

FIGS. 5 and 6 show examples of the analysis report. FIG. 5 shows area information, and the total area is "31387.996094". FIG. 6 shows timing information, and the data arrival time is "-7.70".

The CPU 1 compares the values in the analysis report with pre-input desirable specifications (conditions for design) (ST8). If conditions for timing or layout area of the desirable specifications are not satisfied (area violation), the logic synthesis is executed once again (ST4).

If the conditions for timing and layout area of the desirable specifications are satisfied in step ST8,

the CPU 1 extracts the timing information and layout area information and writes the information in the header portion of the executed RTL description (ST9). The layout area information "31387.996094" gate in the area information shown in FIG. 5 and the timing information "-7.70" ns shown in FIG. 6 are written in the header portion of the RTL description shown in FIG. 3.

The CPU 1 executes a logic simulation for the gate-level net list by the logic simulation tool 5d (ST10). The CPU 1 then inputs the simulation data to the power consumption calculation tool 5d, carries out a power consumption calculation process (ST11) and outputs a power consumption calculation result list (power consumption data) (ST12). In this case, the list may be printed out by the printer 10 or displayed on the display 6.

FIG. 7 shows an example of the power consumption calculation result. In FIG. 7, PowerAVERAGE "5.00071" is a total power consumption.

The CPU 1 extracts power consumption information from the power consumption calculation result list and writes it in the header portion of the executed RTL description (ST13). The power consumption "5.00071" mA in FIG. 7 is written in the header portion of the RTL description in FIG. 3.

At last, the CPU 1 stores the RTL description

comprising the header portion and entity portion, as shown in FIG. 3, at a designated location of the HDD 5 as one file (ST14).

As has been described above, according to the embodiment, the processes of steps ST1-3, 4-9, 10-13 and 14 are automated. Thereby, the reuse design data comprises the header portion (information portion) and the RTL description portion (entity portion) and contains data in the same file. Thus, the reuse design database can easily be managed in a unified manner.

In the above embodiment, the four data items, i.e. simulation time, layout area, timing, and power consumption, are written in the information portion (header portion) of the database. Additionally, other necessary information may be written.

According to the above-described embodiment of the invention, there is no need to consume time in constructing a database after the completion of development of an ASIC, and efficient development can be made.

The management of the database can easily be made by unifying the information portion (header portion) and RTL description portion (entity portion) of the database in the same file.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to

the specific details and representative embodiments shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.